a plurality of internal connection leads formed on said unitary frame body adjacent to said chip-receiving windows and adapted to be connected electrically to bonding pads on the integrated circuit chips in said chip-receiving windows such that internal electrical connection among the integrated circuit chips can be established via said internal connection leads; and

a plurality of external connection leads formed on said unitary frame body adjacent to at least one of said chip-receiving windows and adapted to be connected electrically to the bonding pads on the integrated circuit chip in said at least one of said chip-receiving windows, said external connection leads serving as terminal pins such that external electrical connection with the integrated circuit chip in said at least one of said chip-receiving windows can be established via said external connection leads to provide an individual semiconductor chip package.

2. The lead frame of Claim 1, wherein said internal connection leads are adapted to be wire-bonded to the bonding pads on the integrated circuit chips in said chip-receiving windows.

3. The lead frame of Claim 1, wherein said external connection leads are adapted to be wire-bonded to the bonding pads on the integrated circuit chip in said at least one of said chip-receiving windows.

4. (Amended) A semiconductor chip package comprising:

a lead frame including a unitary frame body and at least two chip-receiving windows formed in said unitary frame body;

at least two integrated circuit chips, each of which is received in a respective one of said chip-receiving windows and has a plurality of bonding pads thereon;

a plurality of internal connection leads formed on said unitary frame body adjacent to said chip-receiving windows, said internal connection leads being connected electrically to said bonding pads on said integrated circuit chips in said chip-receiving windows to establish internal electrical connection among said integrated circuit chips; and

a plurality of external connection leads formed on said unitary frame body adjacent to at least one of said chip-receiving windows, said external connection leads being connected electrically to said bonding pads on said integrated circuit chip in said at least one of said chip-receiving windows, and serving as terminal pins such that external electrical connection with said integrated circuit chip in said at least one of said chip-receiving windows is established via said external connection leads to provide an individual semiconductor chip package.

5. The semiconductor chip package of Claim 4, wherein said internal connection leads

are wire-bonded to said bonding pads on said integrated circuit chips in said chip-receiving windows.

6. The semiconductor chip package of Claim 4, wherein said external connection leads are wire-bonded to said bonding pads on said integrated circuit chip in said at least one of said chip-receiving windows.

7. The semiconductor chip package of Claim 4, wherein said integrated circuit chip in said at least one of said chip-receiving windows is a master integrated circuit chip, and said integrated circuit chip in other ones of said chip-receiving windows is a slave integrated circuit chip.

8. The semiconductor chip package of Claim 7, wherein said master integrated circuit chip includes an embedded testing circuit for testing of said slave integrated circuit chip that is connected thereto.

REMARKS

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

Claims 1-8 are pending, with claims 1 and 4 being amended herein.

The Examiner rejects claims 1-8 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,160,312 to Raad in view of the prior art submitted by applicant in Figure 1. Applicant has carefully considered the Examiner's description of the Raad reference and its combination with Figure 1 of the application, and respectfully believes that the cited references fail to teach or suggest the claimed invention of claims 1-8, particularly in view of the clarifying amendments to independent claims 1 and 4. Raad discloses an embedded memory assembly which is mounting atop a microprocessor with the purpose of increasing the speed of signal transfer between the memory and the microprocessor. As part of the Raad structure, there is provided a frame 109, with internal signal leads 111 upon which a pair of memory devices 103 sit and are electrically connected. The internal signal leads 111 connecting the two memory devices in turn sit on top of electrical vias 201, which are electrically connected to the microprocessor 101. The microprocessor 101 itself has external leads 113. It is thus clear that the Raad reference does not disclose a "unitary frame body" (as is set forth in claims 1 and 4 as amended) but instead teaches two separate structures that lie on different planes. Figure 1 of the instant application